Birzeit University logo

Faculty of Engineering and Technology

Electrical and Computer Engineering Department

Advanced Digital Design ENCS3310

Homework#2

Given the following figure

1. Write a Verilog description for the D Flip-Flop, JK Flip-Flop, and the MUX.
2. Write a Structural Verilog Description for the Circuit using modules in part ‘a’.
3. Derive the state diagram (or state table) for the circuit. Then, write a behavioral Verilog description based on this state diagram.
4. Write a Verilog test bench for the circuit.

(Please submit your code + Screen shots of the simulation).

